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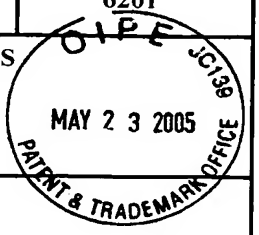
AMENDMENT TRANSMITTAL LETTER (Large Entity)

Applicant(s): **Myun-Joo PARK et al.**

Docket No. **SEC.1067**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/644,735	August 21, 2003	Trong Q. Phan	20987	2827	6201

Invention: **SEMICONDUCTOR MEMORY SYSTEM HAVING MULTIPLE SYSTEM DATA BUSES**



COMMISSIONER FOR PATENTS:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST # PREV. PAID FOR		NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	21	-	21	=	0	x $50.00	$0.00
INDEP. CLAIMS	3	-	3	=	0	x $200.00	$0.00
Multiple Dependent Claims (check if applicable) ☐							$0.00
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT							$0.00

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Dated: **MAY 23, 2005**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent application of	:	**Mail Stop Amendment**
Myun-Joo PARK et al.	:	Group Art Unit 2827
Serial No.: 10/644,735	:	Examiner: PHAN, Trong Q.
Filing Date: August 21, 2003	:	

Title: SEMICONDUCTOR MEMORY SYSTEM HAVING MULTIPLE SYSTEM DATA BUSES

REQUEST FOR RECONSIDERATION

U.S. Patent and Trademark Office
Customer Window, Mail Stop
Randolph Building
401 Dulany Street
Alexandria , VA 22314

Sir:

In the Office Action dated March 23, 2005, claims 1-21 of the present application were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,438,014 to Funaba et al. (hereafter, Funaba). The rejection is respectfully traversed for at least the following reasons.

The Office Action states that Funaba "discloses in Fig. 12 a memory system comprising: memory controller; system memory data wiring BUS having a plurality of data buses...; a plurality of memory modules" (See, Office Action at paragraph 2, lines 3-7). However, Figure 12 in Funaba shows only one (1) data bus connected to

four (4) memory modules. While the data bus may contain multiple data bits (See, Funaba at column 13, lines 21-23), it is still only one (1) bus, not a "plurality of data buses". The disclosure of Funaba also describes a single (1) data bus connected to multiple memory modules: "memory modules are branch connected to a bus on a motherboard" (See, Funaba at col. 13, lines 5-6).

In contrast to Funaba, independent claims 1, 8, and 15 each recite "N system data buses" respectively connected to "N memory modules". Since Funaba does not disclose this feature of independent claims 1, 8, and 15, the rejection of these claims under 35 U.S.C. § 103(a) is unsupported and should be withdrawn. Accordingly, the rejection of dependent claims 2-7, 9-14, and 16-21 is also unsupported and should be withdrawn.

In a related matter, Funaba also fails to disclose memory module groups, wherein each memory module group comprises N modules respectively connected to the N system data buses, as described in independent claims 1 and 15. Likewise, Funaba also fails to "[a] module group having at least one memory module connected to all of the N system data buses" as recited in independent claim 8. Because Funaba does not disclose these features of independent claims 1, 8, and 15, the rejection of these claims under 35 U.S.C. § 103(a) is improper and should be withdrawn. Accordingly, the rejection of dependent claims 2-7, 9-14, and 16-21 is also improper and should be withdrawn.

Finally, it should be noted that Funaba repeatedly states throughout its disclosure that all of its memory modules are connected in serial, or sequential form (See, for example, Funaba at Abstract, lines 10-11 or col. 3, lines 35-36). Such a system has been carefully distinguished in the background section of the present specification with reference to FIG. 1 (See, present specification, paragraphs [0005] and [0006]). As a result, the examiner should be able to readily identify many additional features of the present invention that are distinct from systems such as the one described in Funaba.

As the art of record fails to suggest or disclose multiple elements in the claimed invention, a serious reconsideration of the stated rejection is requested. Applicants submit that pending claims 1-21 are distinct from the art of record and are in condition for allowance.

Respectfully submitted,

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Date: May 23, 2005

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